<u>S/N 09/834,751</u> <u>PATENT</u>

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

 Applicant:
 Sergey A. Velichko et al.
 Examiner: Craig S. Miller

 Serial No.:
 09/834,751
 Group Art Unit: 2857

 Filed:
 April 13, 2001
 Docket: 303.750US1

Title: CONCURRENT CONTROL OF SEMICONDUCTOR PARAMETRIC

TESTING

## COMMUNICATION CONCERNING RELATED APPLICATION(S)

## MS Amendment

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No. 11/342419	Filing Date/Issue Date January 30, 2006	Attorney Docket 303.821US3	Title DYNAMICALLY ADAPTABLE SEMICONDUCTOR PARAMETRIC TESTING
11/342425	January 30, 2006	303.821US4	DYNAMICALLY ADAPTABLE SEMICONDUCTOR PARAMETRIC TESTING
11/265897	November 3, 2005	303.855US2	DYNAMIC CREATION AND MODIFICATION OF WAFER TEST MAPS DURING WAFER TESTING

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, ans is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24 day of April, 2006.

KATE GANNON

Signature